REMARKS

In the September 21, 2004 Office Action, the Examiner noted that claims 1-17 were pending in the application and rejected claims 1-17 under 35 U.S.C. § 103(a). In rejecting the claims, U.S. Patents 5,142,630 to Ishikawa; 4,881,170 to Morisada (References A and B, respectively, in the November 18, 2002 Office Action); 5,442,756 to Grochowski et al. (Reference A in the February 11, 2004 Office Action); and U.S. Patent 5,752,259 to Tran (Reference A in the September 21, 2004 Office Action) were cited. Claims 1-17 remain in the case. The Examiner's rejections are traversed below.

The September 21, 2004 Office Action rejected the claims using the same references as in the February 11, 2004 Office Action, except for the addition of Tran as a tertiary reference to reject most of the claims and as the secondary reference used to reject claims 11 and 16, instead of Shiell et al. and Grochowski et al. Therefore, the differences between the present invention and the features allegedly taught by Tran will be discussed below.

A microprocessor with an instruction cache is disclosed by Tran that "supports out-of-order execution, and employs reorder buffer 32 for storing execution results of speculatively-executed instructions and storing these results into register file 34 in program order" (column 8, lines 17-20). The instructions are obtained by concurrently using a plurality of instruction fetch addresses. The microprocessor taught by Tran has reservation stations and a branch prediction mechanism for executing instructions out of order. However, nothing has been cited or found regarding instruction fetch control for a branch instruction based on address mode information.

In paragraphs 3-48 on pages 2-23 of the Office Action, claims 1-3, 5, 6, 8-10, 12-15 and 17 were rejected under 35 USC § 103(a) as unpatentable over Ishikawa in view of Grochowski et al. and Tran. As discussed in the Amendment filed June 14, 2004, Ishikawa and Grochowski et al. do not teach anything related to "instruction execution by way of an out-of-order system" (claim 1, line 3). Although Tran discloses a microprocessor related to the preamble of the independent claims, neither Tran nor any of the previously-cited references teach or suggest "storing a combination of address mode information of a fetched instruction and an instruction address of the fetched instruction" (claim 1, lines 4-5) or "transferring the address mode information ... to the branch instruction control circuit when the branch instruction is executed" (claim 1, lines 12-13), so that the branch instruction can use "the address mode information .... as a branch destination of the branch instruction if the branch instruction is not accompanied by an address mode change" (claim 1, last three lines).

In the exemplary embodiment described on pages 29-36 with reference to Figs. 8-12 of the application, the term "address mode" refers to the size of the address space, i.e., whether the address is 24 bits or 31 bits. No suggestion has been cited or found in Tran of different address modes or sizes of the address space being taken into account by an out-of-order execution system. Since neither Ishikawa, nor Grochowski et al. contain any mention of an out-of-order execution system, the combination of these three references lack any suggestion of how an out-of-order execution system could take different address modes, or address space sizes into account.

For example, nothing has been cited or found in Ishikawa or Grochowski et al. of "storing a combination of address mode information of a fetched instruction and an instruction address of the fetched instruction" (claim 1, lines 4-5). By storing this combination of information, the present invention enables each of the instructions in an execution pipeline or an instruction fetch pipeline to correctly acquire a relevant address space even if the address mode information of the instructions are different. In Ishikawa, the relevant address space of an instruction to be executed next is acquired only as a result of executing an instruction (a BSM or BASSM instruction) and therefore, the instruction execution sequence cannot be changed if the address space changes.

The deficiencies of Ishikawa and Tran are not overcome by Grochowski et al., since it only describes controlling a branch instruction using a branch prediction mechanism and is not related to either an out-of-order pipeline execution system, or a microprocessor that has different address modes (address spaces). Thus, combining Ishikawa and Grochowski et al. with Tran might result in a method for predicting a branch destination address of a BSM or BASSM instruction in an instruction pipeline capable of out-of-order execution, but there would be no capability of handling changes in the instruction address space, so that instruction fetches are performed correctly.

The inclusion of a storage circuit, branch instruction control circuit and transfer circuit that perform the operations recited in claim 1 with regard to address mode information and an instruction pipeline operated by way of an out-of-order system provides the benefit of controlling execution of an instruction fetch control unit in an execution pipeline for an instruction sequence of different instruction spaces.

A concrete example may help in understanding how the present invention differs from the prior art. In the case of an instruction address near the maximum range of the smaller of two address spaces, e.g., the 16MB address space associated with a 24-bit address, when instruction execution is performed sequentially, the address of the next instruction to be executed is different depending upon whether the address mode is 24 bits or 31 bits.

For the above reasons, it is submitted that claim 1 and claims 2, 3, 5, 6, and 8 which depend therefrom, patentably distinguish over Ishikawa in view of Grochowski et al. and Tran. Limitations similar to those discussed above with respect to claim 1 are recited in claims 9, 10, 12-15 and 17. Therefore, it is submitted that claims 9, 10, 12-15 and 17 patentably distinguish over these three references for the reasons discussed above with respect to claim 1.

In paragraphs 49-51 on pages 23-25 of the Office Action, claims 4 and 7 were rejected as unpatentable over Ishikawa in view of Grochowski et al. and Tran and further in view of Morisada. Nothing has been cited or found in Morisada teaching or suggesting modification of Ishikawa, Grochowski et al., and Tran to overcome the deficiencies discussed above. Since claims 4 and 7 depend from claim 1, it is submitted that claims 4 and 7 patentably distinguish over Ishikawa in view of Grochowski et al., Tran and Morisada for the reasons discussed above with respect to claim 1.

In paragraphs 52-56 on pages 25 and 26 of the Office Action, claims 11 and 16 were rejected under 35 USC § 103(a) as unpatentable over Ishikawa in view of Tran. Claim 11 recites "storing a combination of mode information of an instruction to be fetched and an instruction address of the instruction ... in ... [an] out-of-order system" (claim 11, lines 4-7) and "performing an instruction pre-fetch of a branch destination of a branch instruction based on mode information corresponding to a second port of the instruction fetch ports by way of the out-of-order system" (claim 11, lines 8-9). Since similar limitations are recited in claim 16, it is submitted that claims 11 and 16 patentably distinguish over Ishikawa in view of Tran for the reasons discussed above with respect to limitations similar to those quoted in this paragraph.

Summary

It is submitted that the references cited by the Examiner, taken individually or in combination, do not teach or suggest the features of the present claimed invention. Thus, it is submitted that claims 1-17are in a condition suitable for allowance. Reconsideration of the claims and an early Notice of Allowance are earnestly solicited.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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